



Accelerating XOR-Based Erasure Coding using Program Optimization Techniques Yuya Uezato DWANGO, Co., Ltd.

Optimizing matrix multiplication over two finite fields:

(for Standard EC)
$$A \times B$$
 over $\mathbb{F}[2^8]$,
(for XOR-based EC) $C \times D$ over $\mathbb{F}[2]$.

Byte Finite Field \$\mathbb{F}[2^8]\$ is a field with 256 elements.
Bit Finite Field \$\mathbb{F}[2] = {0,1}\$ is a field with the two bits.

What we need to know about $\mathbb{F}[2^8]$ and $\mathbb{F}[2]$.

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- $\mathbb{F}[2^8]$ is a field with $2^8 = 256$ elements.
 - ★ 1-byte (8-bits) data can be seen as an element of $\mathbb{F}[2^8]$._____
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Byte



- $\mathbb{F}[2] = \{0, 1\}$ is a field of bits.
 - \blacktriangleright Its addition is XOR \oplus .
 - ► Its multiplication is AND &.
 - \blacktriangleright 0 and 1 satisfy the following:

$$x\oplus 0=0\oplus x=x,\quad y\&1=1\&y=y.$$

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$$\begin{array}{c|c} 10 & 1 & 1 \\ 14 & A & \times_{\mathbb{F}[2^8]} & 10 & B \end{array}$$

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$$\frac{10}{14} \times_{\mathbb{F}[2^8]} \frac{10 - 4M}{10}$$

This setting comes from *erasure coding*.

What are Erasure Coding (EC) and XOR-Based EC

Example (Building a streaming media server with criteria)

- 1. We have 14 nodes. Each node has a 20TB disk.
- 2. We can load data even if nodes ≤ 4 are down.
- 3. The total capacity of our server = 200TB.
 - ▶ $14 \cdot 20 200 = 80$ TB can be used for data redundancy.

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For this criteria, we can employ Reed-Solomon EC RS(d = 10, p = 4). *d*: we can assume *d*-nodes are living. (d = 14 − p = 10). *p*: we can permit nodes

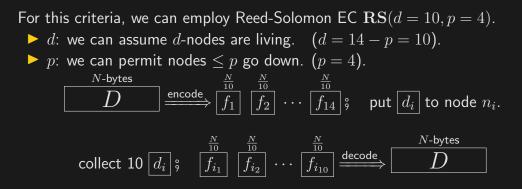
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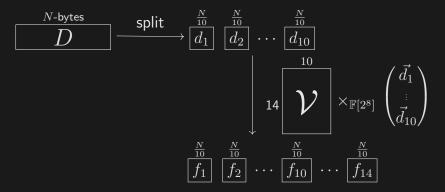
For this criteria, we can employ Reed-Solomon EC $\mathbf{RS}(d = 10, p = 4)$. $\blacktriangleright d$: we can assume *d*-nodes are living. (d = 14 - p = 10). $\blacktriangleright p$: we can permit nodes $\leq p$ go down. (p = 4). $\square D \longrightarrow \stackrel{N-bytes}{\longrightarrow} \stackrel{N}{f_1} \stackrel{N}{f_2} \cdots \stackrel{N}{f_{14}} \stackrel{n}{\circ} \text{ put } d_i$ to node n_i .

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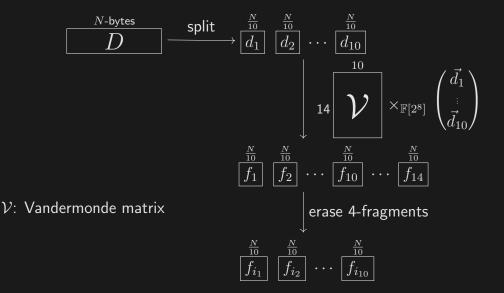
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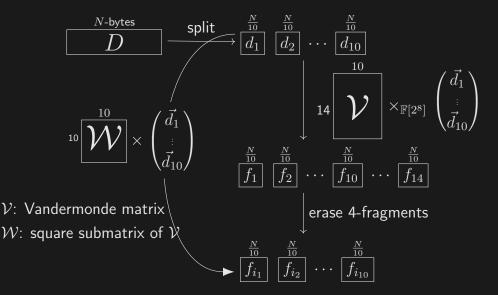


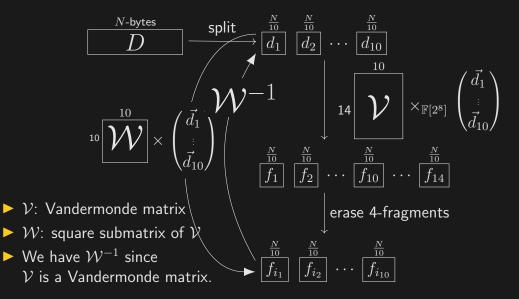


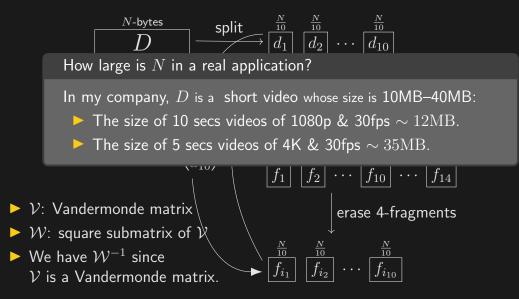


V: Vandermonde matrix









$\mathsf{Optimizing}\,\,\mathcal{V}\times_{\mathbb{F}[2^8]}D$

Q. What is the heaviest operation on $\mathcal{V} \times_{\mathbb{F}[2^8]} D$? A. Multiplication of $\mathbb{F}[2^8]$:

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• Internally, $p \in \mathbb{F}[2^8]$ is a 7-degree polynomial over $\mathbb{F}[2]$:

 $b_7x^7 + \overline{b_6x^6 + \dots + b_1x + b_0}$ where $\overline{b_i \in \mathbb{F}[2]}$.

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▶ p₁ + p₂ of 𝔅[2⁸] is the polynomial addition. Easy because just componentwise XOR:

$$(b_7 \oplus b'_7)x^7 + (b_6 \oplus b'_6)x^6 + \dots + (b_0 \oplus b'_0).$$

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1. We do the 7-degree polynomial multiplication p₁ × p₂.
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XOR-based EC is one way to vanish \cdot of $\mathbb{F}[2^8]$.

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There is an injective ring homomorphism $\mathcal{B} : \mathbb{F}[2^8] \to 8 \boxed{\mathbb{F}[2]}$ I.e.,
 $\forall x, y \in \mathbb{F}[2^8]$.
 $\begin{cases} x + y = \mathcal{B}^{-1}(\mathcal{B}(x) + \mathcal{B}(y)), \\ x \cdot y = \mathcal{B}^{-1}(\mathcal{B}(x) \times \mathcal{B}(y)) \end{cases}$

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Prop: Emulate $\mathcal{W}^{-1} \times (\mathcal{W} \times D) = D$ in the $\mathbb{F}[2]$ world

$$\mathcal{B}(\mathcal{W}^{-1}) \stackrel{\mathbb{F}[2]}{\times} (\mathcal{B}(\mathcal{W}) \stackrel{\mathbb{F}[2]}{\times} \widetilde{D}) = \mathcal{B}(\mathcal{W}^{-1} \times \mathcal{W}) \times \widetilde{D} = \widetilde{D}.$$

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 $\begin{pmatrix} x_1 & x_2 \\ x_3 & x_4 \end{pmatrix} \times_{\mathbb{F}[2^8]} \begin{pmatrix} d_1 & \cdots \\ d_2 & \cdots \end{pmatrix} = \begin{pmatrix} x_1 \cdot d_1 + x_2 \cdot d_2 & \cdots \\ x_3 \cdot d_1 + x_4 \cdot d_4 & \cdots \end{pmatrix}$
 \downarrow
 $\begin{pmatrix} 1 & 1 & 0 & 1 & \cdots \\ 0 & 1 & 1 & 0 & \cdots \\ 1 & 0 & 0 & 1 & \cdots \end{pmatrix} \times_{\mathbb{F}[2]} \begin{pmatrix} \vec{x}_1 \\ \vec{x}_2 \\ \vec{x}_3 \\ \vec{x}_4 \end{pmatrix} = \begin{pmatrix} \vec{x}_1 \oplus \vec{x}_2 \oplus \vec{x}_4 \oplus \cdots \\ \vec{x}_2 \oplus \vec{x}_3 \oplus \cdots \\ \vec{x}_1 \oplus \vec{x}_4 \oplus \cdots \end{pmatrix}$

 \oplus is byte-array XOR.

Comparing MM over $\mathbb{F}[2^8]$ and MM over $\mathbb{F}[2]$ for Encoding

Trade-off in Matrix Multiplication	$\mathbf{RS}(10,4)$ by $\mathbb{F}[2^8]$	$\mathbf{RS}(10,4)$ by $\mathbb{F}[2]$
Number of Core Operation	$\mathcal{V}:$ 14 $\mathbb{F}[2^8]$	$\mathcal{B}(\mathcal{V}):$ 112 $\mathbb{F}[2]$
Speed of Core Operation	+ of $\mathbb{F}[2^8]$ is fast \cdot of $\mathbb{F}[2^8]$ is slow	bytevec-XOR \oplus is fast (SIMDable)

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Encoding Throughput Comparison (on Intel CPU):				
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/	$ $ ISA-L [‡] $\mathbb{F}[2^8]$	State-of-the-art ${}^{lacksymbol{ heta}} \mathbb{F}[2]$	
RS(10, 4)	6.79	4.94	
RS(10, 3)	6.78	6.15	
RS(10, 4) RS(10, 3) RS(9, 3)	7.31	6.17	

ISA-L: Intel's EC library https://github.com/intel/isa-1
 T. Zhou & C. Tian. 2020. Fast Erasure Coding for Data Storage: A Comprehensive Study of the Acceleration Techniques.

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Our Contribution:

Optimizing Bitmatrix Multiplication

as

Program Optimization Problem

MM over $\mathbb{F}[2] = \mathsf{Running Straight Line Program}$

We identify bitmatrix multiplication as *straight line program* (SLP):

$$\begin{pmatrix} 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 0 & 1 & 1 & 1 \end{pmatrix} \times_{\mathbb{F}[2]} \begin{pmatrix} \vec{a} \\ \vec{b} \\ \vec{c} \\ \vec{d} \end{pmatrix}$$
$$\underbrace{P(a, b, c, d)}_{v_1 \leftarrow a \oplus b; \\ v_2 \leftarrow a \oplus b \oplus c; \\ v_3 \leftarrow b \oplus c \oplus d; \\ \mathsf{return}(v_1, v_2, v_3)$$

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 \star "Bitmatrix as SLP" is not a new idea (See. Boyar+ 2008)

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★ "Bitmatrix as SLP" is not a new idea (See. Boyar+ 2008)
▶ SLP only allow assignments with one kind *binary* operator ⊕.
▶ SLP do not have functions, if-branchings, and while-loop, etc.

Optimization Metric $\#_{\oplus}(_)$: the number of XORs.

Q

$$\begin{array}{ccc}
P & \#_{\oplus} = 8 \\
\hline
v_1 \leftarrow a \oplus b; \\
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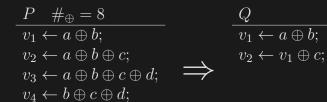
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$$\begin{array}{cccc}
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\hline
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v_2 \leftarrow a \oplus b \oplus c; \\
v_3 \leftarrow a \oplus b \oplus c \oplus d; & \Longrightarrow \\
v_4 \leftarrow b \oplus c \oplus d; & & & \\
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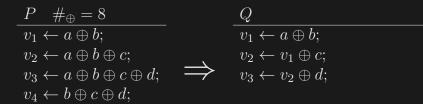
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 $\oplus d$.

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Optimization Metric $\#_{\oplus}(_)$: the number of XORs.

return (v_1, v_2, v_3, v_4)

P and Q are equivalent: [[P]] = [[Q]].
Intuitively, Q (#⊕(Q) = 4) runs faster than P (#⊕(P) = 8).

Optimization Metric $\#_{\oplus}(_)$: the number of XORs.

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 \triangleright P and Q are equivalent: $\llbracket P \rrbracket = \llbracket Q \rrbracket$. Intuitively, Q ($\#_{\oplus}(Q) = 4$) runs faster than P ($\#_{\oplus}(P) = 8$). Question. For a given SLP P, can we quickly find the most efficient equivalent SLP Q?

Optimization Metric $\#_{\oplus}(_)$: the number of XORs.

 $\mathsf{return}(v_1, v_2, v_3, v_4)$

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Theorem (Boyar+ 2013)

Unless $\mathbf{P} = \mathbf{NP}$, for a given SLP P, in polynomial time, we cannot find Q such that $\llbracket P \rrbracket = \llbracket Q \rrbracket$ and minimizes $\#_{\oplus}(Q)$.

Our Heuristic: Grammar Compression Algorithm RePAIR

Originally, RePair is an algorithm to compress context-free grammars. We use it identifying SLPs as commutative CFGs.

- Larsson & Moffat. 1999. Offline dictionary-based compression
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 REPAIR = Repeat PAIR. The key operation is PAIR:

$$\begin{array}{c} v_{1} \leftarrow a \oplus b; \\ v_{2} \leftarrow a \oplus b \oplus c; \\ v_{3} \leftarrow a \oplus b \oplus c \oplus d; \\ v_{4} \leftarrow b \oplus c \oplus d; \\ \#_{\oplus} = 8 \end{array} \xrightarrow{PAIR(\mathbf{a}, \mathbf{c})} \begin{array}{c} t_{1} \leftarrow a \oplus c; \\ v_{1} \leftarrow a \oplus b; \\ v_{1} \leftarrow a \oplus b; \\ v_{2} \leftarrow t_{1} \oplus b; \\ v_{3} \leftarrow t_{1} \oplus b \oplus d; \\ v_{4} \leftarrow b \oplus c \oplus d; \end{array}$$

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How do we choose a pair of terms to do pairing?

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How do we choose a pair of terms to do pairing? Greedy.

$$\begin{array}{c} v_1 \leftarrow \mathbf{a} \oplus \mathbf{b}; \\ v_2 \leftarrow \mathbf{a} \oplus \mathbf{b} \oplus \mathbf{c}; \\ v_3 \leftarrow \mathbf{a} \oplus \mathbf{b} \oplus \mathbf{c} \oplus \mathbf{d}; \end{array} \xrightarrow{\text{PAIR}(\mathbf{a}, \mathbf{b})} \underbrace{\begin{array}{c} t_1 \leftarrow \mathbf{a} \oplus \mathbf{b}; \\ v_2 \leftarrow t_1 \oplus \mathbf{c}; \\ v_3 \leftarrow t_1 \oplus \mathbf{c} \oplus \mathbf{d}; \end{array} }_{v_4 \leftarrow \mathbf{b} \oplus \mathbf{c} \oplus \mathbf{d};} \#_{\oplus} = 6 \end{array}$$

Our Heuristic: Grammar Compression Algorithm REPAIR

Originally, RePAIR is an algorithm to compress context-free grammars. We use it identifying SLPs as commutative CFGs.

Larsson & Moffat. 1999. Offline dictionary-based compression
 Paar. 1997. Optimized arithmetic for Reed-Solomon encoders
 REPAIR = Repeat PAIR. The key operation is PAIR:

 $v_1 \leftarrow a \oplus b$: $t_1 \leftarrow a \oplus c;$ $\begin{array}{c} v_2 \leftarrow a \oplus b \oplus c; \\ v_3 \leftarrow a \oplus b \oplus c \oplus d; \end{array} \xrightarrow{\text{PAIR}(\mathbf{0}, \mathbf{C})} \overbrace{v_1 \leftarrow a \oplus b; \\ v_2 \leftarrow t_1 \oplus b;} v_2 \leftarrow t_1 \oplus b; \end{array} \qquad \#_{\oplus} = 7$ $v_4 \leftarrow b \oplus c \oplus d;$ $v_3 \leftarrow t_1 \oplus b \oplus d$: $v_4 \leftarrow b \oplus c \oplus d$: $\#_{\oplus} = 8$ $t_1 \leftarrow a \oplus b;$ $t_1 \leftarrow a \oplus b;$ $t_1 \leftarrow a \oplus b;$ $t_2 \leftarrow t_1 \oplus c$: $v_3 \leftarrow t_2 \oplus d;$ $v_{A} \leftarrow b \oplus c \oplus d$: $v_{A} \leftarrow b \oplus c \oplus d$: $v_4 \leftarrow t_3 \oplus d$:

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The commutative version of REPAIR accommodates

Commutativity : $x \oplus y = y \oplus x$, Associativity : $(x \oplus y) \oplus z = x \oplus (y \oplus z)$. In the paper, we extend it to XORREPAIR by accommodating

Cancellativity: $x \oplus x \oplus y = y$.

Optimization Metric: $\#_{mem}(_{-}) =$ the number of memory access.

Quiz: How many times will this program access memory?

$$\#_{\mathsf{mem}} \left(v \leftarrow A \oplus B \oplus C \oplus D \right) = ?$$

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$$\#_{\mathsf{mem}} \left(v \leftarrow A \oplus B \oplus C \oplus D \right) = 9$$

because each \oplus issues two read and one write:

$$t_1 \leftarrow A \oplus B; \quad t_2 \leftarrow t_1 \oplus C; \quad v \leftarrow t_2 \oplus D;$$

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$$t_1 \leftarrow A \oplus B; \quad t_2 \leftarrow t_1 \oplus C; \quad v \leftarrow t_2 \oplus D;$$

 t_1 and t_2 are wasteful: they are released immediately after allocated.

To reduce such wastefulness, we extend SLP to MultiSLP, which allows n-arity XORs.

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because each \oplus issues two read and one write:

$$t_1 \leftarrow A \oplus B; \quad t_2 \leftarrow t_1 \oplus C; \quad v \leftarrow t_2 \oplus D;$$

On MultiSLP, we can

 $v \leftarrow \oplus_4(A, B, C, D);$

Thus, we have $\#_{mem} = 5$.

 $\begin{array}{l} \oplus_4(A, \ B, \ C, \ D: \ [byte]) \ \{ \\ var \ v = \ Array::new(A.len); \\ for \ i \ in \ [0..A.len): \\ byte \ r = \ A[i] \ ^ B[i] \\ r = r \ ^ C[i]; \\ v[i] = r \ ^ D[i]; \\ return \ v; \\ \} \end{array}$

New Metric and Memory Optimization Problem

From a given P, can we quickly (= in polynomial time) find an equivalent and most memory efficient Q w.r.t. $\#_{mem}$?

$$P: \begin{array}{l} v_1 \leftarrow a \oplus b \oplus c \oplus d \oplus e; \\ v_2 \leftarrow a \oplus b \oplus c \oplus d \oplus f; \\ \#_{\mathsf{mem}}(P) = 24 \end{array}$$

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Unfortunately, we showed the following intractability result:

Theorem (Our NEW theoretical result) Unless $\mathbf{P} = \mathbf{NP}$, for a given SLP P, in polynomial time, we cannot find Q that $[\![P]\!] = [\![Q]\!]$ and minimizes $\#_{mem}(Q)$.

$$\begin{array}{c} \boldsymbol{\alpha} \leftarrow \oplus(x_1, \dots, x_n); \\ \vdots \\ \beta \leftarrow \oplus(y_1, \dots, \boldsymbol{\alpha}, \dots, y_m) \end{array} \xrightarrow{\text{fuse}} \beta \leftarrow \oplus(y_1, \dots, x_1, \dots, x_n, \dots, y_m) \\ \stackrel{\boldsymbol{\alpha}}{\prec} \alpha \text{ appears once in the program} \end{array}$$

1

$$\begin{array}{cccc} \boldsymbol{\alpha} \leftarrow \oplus(x_{1}, \dots, x_{n}); \\ \vdots & & \text{fuse} \\ \beta \leftarrow \oplus(y_{1}, \dots, \boldsymbol{\alpha}, \dots, y_{m}) \\ \Rightarrow & \alpha \text{ appears once in the program} \end{array} \\ \begin{array}{c} \textbf{Example.} & & \textbf{t}_{1} \leftarrow a \oplus b; \\ t_{2} \leftarrow a \oplus b \oplus c \oplus d \oplus f; \\ t_{2} \leftarrow a \oplus b \oplus c \oplus d \oplus f; \\ \#_{\text{mem}}(24) \end{array} & \begin{array}{c} \textbf{t}_{1} \leftarrow a \oplus b; \\ t_{2} \leftarrow t_{1} \oplus c; \\ t_{3} \leftarrow t_{2} \oplus d; \\ v_{1} \leftarrow t_{3} \oplus e; \\ v_{2} \leftarrow t_{3} \oplus f; \\ \#_{\text{mem}}(15) \end{array} & \begin{array}{c} t_{2} \leftarrow \oplus_{3}(a, b, c); \\ t_{2} \leftarrow \oplus_{3}(a, b, c); \\ t_{2} \leftarrow \oplus_{3}(a, b, c); \\ t_{3} \leftarrow t_{2} \oplus d; \\ v_{1} \leftarrow t_{3} \oplus e; \\ v_{2} \leftarrow t_{3} \oplus f; \\ \#_{\text{mem}}(13) \end{array} \end{array}$$

1

$$\begin{array}{c} \mathbf{\alpha} \leftarrow \oplus(x_1, \dots, x_n); \\ \vdots \\ \beta \leftarrow \oplus(y_1, \dots, \mathbf{\alpha}, \dots, y_m) \\ \Rightarrow \alpha \text{ appears once in the program} \\ \hline \mathbf{Example.} \\ 1 \leftarrow a \oplus b \oplus c \oplus d \oplus e; \\ 2 \leftarrow a \oplus b \oplus c \oplus d \oplus f; \\ \# \operatorname{mem}(24) \\ \hline \mathbf{fuse}(i_2) \\ \hline \mathbf{fuse}(i_2) \\ \hline \mathbf{fuse}(i_2) \\ \hline \mathbf{fuse}(i_2) \\ \hline \mathbf{fuse}(11) \end{array} \xrightarrow{\mathbf{fuse}(x_1, \dots, x_n, \dots, y_m)} \xrightarrow{\mathbf{fuse}(x_1, \dots, x_n, \dots, y_m)} \xrightarrow{\mathbf{fuse}(x_1, \dots, x_n, \dots, y_m)} \xrightarrow{\mathbf{fuse}(x_1, \dots, x_1, \dots, x_n, \dots, y_m)} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_m} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_m} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_m)} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_m} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_m} \xrightarrow{\mathbf{fus}(x_1, \dots, x_1, \dots, x_n, \dots, y_n, \dots, y_n} \xrightarrow{\mathbf{fus}(x_1, \dots, x_n, \dots, y_n, \dots, y_n, \dots, y_n} \xrightarrow{\mathbf{fus}(x_1, \dots,$$

$$\begin{array}{cccc} \mathbf{\alpha} \leftarrow \oplus (x_1, \dots, x_n); \\ \vdots & & \text{fuse} \\ \beta \leftarrow \oplus (y_1, \dots, \mathbf{\alpha}, \dots, y_m) \\ \stackrel{\wedge}{\Rightarrow} \alpha \text{ appears once in the program} \\ \hline \\ \textbf{Example.} & & t_1 \leftarrow a \oplus b; \\ t_2 \leftarrow a \oplus b \oplus c \oplus d \oplus e; \\ g \leftarrow a \oplus b \oplus c \oplus d \oplus f; \\ \#_{\text{mem}}(24) & & t_2 \leftarrow t_1 \oplus c; \\ \#_{\text{mem}}(24) & & t_1 \leftarrow t_3 \oplus e; \\ \psi_1 \leftarrow t_3 \oplus e; \\ \psi_2 \leftarrow t_3 \oplus f; \\ \#_{\text{mem}}(11) & & \text{NOT fuse}(t_k) \text{ by } \Rightarrow \\ \hline \\ \textbf{w}_1 \leftarrow \oplus (t_2) & \psi_1 \leftarrow t_3 \oplus e; \\ \psi_2 \leftarrow t_3 \oplus f; \\ \psi_2 \leftarrow \psi_3 \oplus f; \\ \#_{\text{mem}}(12) & & \text{total states} \\ \hline \\ \textbf{w}_1 \leftarrow \psi_2 \leftarrow \psi_3 \oplus \psi_3 & \psi_1 \leftarrow \psi_3 \oplus \psi_3 \\ \psi_2 \leftarrow \psi_3 \oplus \psi_3 & \psi_1 \leftarrow \psi_3 \oplus \psi_3 & \psi_3 \end{pmatrix} \\ \begin{array}{c} \textbf{w}_1 \leftarrow \psi_2 \oplus (t_3) & \textbf{w}_2 \leftarrow \psi_3 \oplus \psi_3 \\ \psi_2 \leftarrow \psi_3 \oplus \psi_3 & \psi_3 \oplus \psi_3 & \psi_3 \end{pmatrix} \\ \hline \\ \textbf{w}_1 \leftarrow \psi_2 \oplus \psi_3 \oplus \psi_3 & \psi_3 \oplus \psi_3 \oplus \psi_3 & \psi_3 \oplus \psi_3 \oplus \psi_3 \oplus \psi_3 \oplus \psi_3 \end{pmatrix} \\ \hline \\ \textbf{w}_1 \leftarrow \psi_2 \oplus \psi_3 \oplus \psi$$

Metric $\#_{I/O}(K, _)$: the total number of I/O transfers between memory and f cache of K-capacity.

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We have three kinds of operations for cache:

- ▶ $\mathcal{H}(x)$: Cache Hit for an element x. $\#_{I/O} = 0$.
- ▶ $\mathcal{R}(x)$: Cache miss. Evict LRU to mem. and read x from mem. $\#_{I/O} = 2$.
- \triangleright $\mathcal{W}(x)$: Cache miss. Evict LRU to mem. and write x to cache. $\#_{1/O} = 1$.

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Example: Calculate $\#_{I/O}(4, P)$ for the following example SLP P:

 $v_1 \leftarrow A \oplus B; \quad \hline \qquad *_1 *_2 *_3 *_4$

 $v_2 \leftarrow \oplus(E, D, A);$

 $v_3 \leftarrow v_1 \oplus E;$

 $v_4 \leftarrow v_1 \oplus C;$ <u>retu</u>rn $(v_2, v_3, v_4);$

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 $v_{1} \leftarrow A \oplus B; \qquad *_{1} *_{2} *_{3} *_{4} \xrightarrow{\mathcal{R}(A)}{2} *_{2} *_{3} *_{4}A$ $v_{2} \leftarrow \oplus (E, D, A); \qquad \\v_{3} \leftarrow v_{1} \oplus E; \qquad \\v_{4} \leftarrow v_{1} \oplus C; \qquad \\\mathsf{return}(v_{2}, v_{3}, v_{4}); \qquad \\$

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$$v_{2} \leftarrow \oplus (E, D, A); \qquad v_{3} \leftarrow v_{1} \oplus E;$$

$$v_{4} \leftarrow v_{1} \oplus C; \qquad \text{return}(v_{2}, v_{3}, v_{4}):$$

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<u>return</u> $(v_2, v_3, v_4),$

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$$v_{2} \leftarrow \oplus (E, D, A); \quad *_{4}ABv_{1}$$

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$$\begin{array}{lll} v_{1} \leftarrow A \oplus B; & *_{1} *_{2} *_{3} *_{4} & \frac{\mathcal{R}(A)}{2} & *_{2} *_{3} *_{4}A & \frac{\mathcal{R}(B)}{2} & *_{3} *_{4}AB & \frac{\mathcal{W}(v_{1})}{1} \\ v_{2} \leftarrow \oplus(E, D, A); & *_{4}ABv_{1} & \frac{\mathcal{R}(E)}{2} & ABv_{1}E & \frac{\mathcal{R}(D)}{2} & Bv_{1}ED & \frac{\mathcal{R}(A)}{2} & v_{1}EDA & \frac{\mathcal{W}(v_{2})}{1} \\ v_{3} \leftarrow v_{1} \oplus E; & EDAv_{2} & \frac{\mathcal{R}(v_{1})}{2} & DAv_{2}v_{1} & \frac{\mathcal{R}(E)}{2} & Av_{2}v_{1}E & \frac{\mathcal{W}(v_{3})}{1} \\ v_{4} \leftarrow v_{1} \oplus C; & v_{2}v_{1}Ev_{3} & \frac{\mathcal{H}(v_{1})}{0} & v_{2}Ev_{3}v_{1} & \frac{\mathcal{R}(C)}{2} & Ev_{3}v_{1}C & \frac{\mathcal{W}(v_{4})}{1} \\ \end{array} \\ \mathbf{return}(v_{2}, v_{3}, v_{4}); & v_{3}v_{1}Cv_{4} \Longrightarrow \#_{\mathbf{I}/\mathbf{O}}(4, P) = 20. \end{array}$$

First approach: Register Assignment

Idea: Reducing the number of variables can relax the pressure of cache, and thus may reduce $\#_{I/O}$.

We do Recycling variables by Register assignment.

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We do Recycling variables by Register assignment.

 $v_1 \leftarrow A \oplus B;$ [5] Register $v_1 \leftarrow A \oplus B;$ [5] #I/O $\begin{array}{ccc} v_2 \leftarrow \oplus(E, D, A); & [7] \\ v_3 \leftarrow v_1 \oplus E; & [5] \end{array} \xrightarrow{\text{assignment}} \end{array}$ $v_2 \leftarrow \oplus(E, D, A); \quad [7]$ $\xrightarrow{v_1 \leftarrow v_1 \oplus C;} \begin{array}{c} v_2 \leftarrow v_2 \oplus (2, 2, 2, 3, 3), \quad [1] \\ v_3 \leftarrow v_1 \oplus E; \quad [5] \\ v_1 \leftarrow v_1 \oplus C; \quad [2] \end{array}$ $v_4 \leftarrow v_1 \oplus C;$ [3] return $(v_2, v_3, v_4);$ return (v_2, v_3, v_1) ; $\xrightarrow[]{\mathcal{R}(v_1)}{0} v_2 E v_3 v_1 \xrightarrow[]{\mathcal{R}(C)}{2} E v_3 v_1 C \xrightarrow[]{\mathcal{W}(v_4)}{1} v_3 v_1 C v_4$ $\begin{array}{c} \xrightarrow{\mathcal{R}(v_1)} & & & \\ \xrightarrow{\mathcal{R}(v_1)} & v_2 E v_3 v_1 \xrightarrow{\mathcal{R}(C)} & E v_3 v_1 \end{array} \xrightarrow{\mathcal{R}(v_1)} & E v_3 C v_1 \end{array}$

It works, but the effect is so limited.

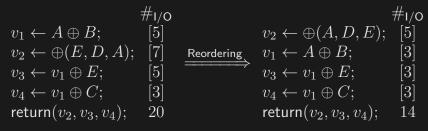
Next Approach: Reordering Statements and Arguments

No side effects on SLPs; thus, we can reorder statements and arguments.



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Using *Pebble Game*, we can integrate {

Recycling Variables and Reordering

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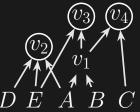
No side effects on SLPs; thus, we can reorder statements and arguments.

#i/o #ı/o $v_1 \leftarrow A \oplus B;$ $v_2 \leftarrow \oplus (A, D, E);$ $\left[5\right]$ [5] $v_2 \leftarrow \oplus (E, D, A); [7]$ $v_1 \leftarrow A \oplus B;$ [3]Reordering $v_3 \leftarrow v_1 \oplus E;$ [5] $v_3 \leftarrow v_1 \oplus E;$ [3] $v_4 \leftarrow v_1 \oplus \overline{C};$ [3] $v_4 \leftarrow v_1 \oplus C;$ [3]return $(v_2, v_3, v_4);$ return $(v_2, v_3, v_4);$ 2014

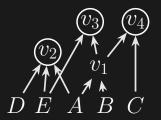
Using *Pebble Game*, we can integrate

- ★ R. Sethi, 1975, Complete register allocation problems.
- We play the pebble game on DAGs or abstract syntax graphs.
- We aim to put pebbles in return nodes.

Recycling Variables and Reordering

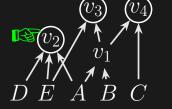


Playing Pebble Game = Deciding Evaluation Order + Variable Recycling



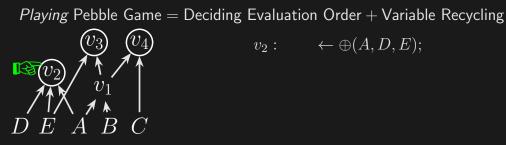
Playing Pebble Game = Deciding Evaluation Order + Variable Recycling

 v_2 :

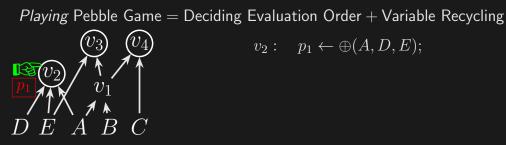


Example: Evaluating strategy based on Depth-first-search

1. Choose v_2 from unvisited roots: alphabetical small $v_2 \prec v_3 \prec v_4$.



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Playing Pebble Game = Deciding Evaluation Order + Variable Recycling

 $v_2: p_1 \leftarrow \oplus(A, D, E);$

$$v_3: \leftarrow E \in$$

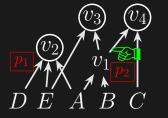
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E A B C

4. Choose v_3 from 2 unvisited roots, and first visit E.

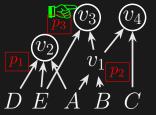
Playing Pebble Game = Deciding Evaluation Order + Variable Recycling



$$v_2: \quad p_1 \leftarrow \oplus (A, D, E); v_1: \quad p_2 \leftarrow A \oplus B; v_3: \quad \leftarrow E \oplus$$

- 1. Choose v_2 from unvisited roots: alphabetical small $v_2 \prec v_3 \prec v_4$.
- 2. Evaluate the children of v_2 in alphabetical order.
- 3. Put a pebble p_1 on v_2 to denote v_2 is visited.
- 4. Choose v_3 from 2 unvisited roots, and first visit E.
- 5. Visit the unvisited child v_1 of v_3 , evaluate, and pebble p_2

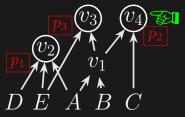
Playing Pebble Game = Deciding Evaluation Order + Variable Recycling



$$v_2: \quad p_1 \leftarrow \oplus (A, D, E); v_1: \quad p_2 \leftarrow A \oplus B; v_3: \quad p_3 \leftarrow E \oplus p_2;$$

- 1. Choose v_2 from unvisited roots: alphabetical small $v_2 \prec v_3 \prec v_4$.
- 2. Evaluate the children of v_2 in alphabetical order.
- 3. Put a pebble p_1 on v_2 to denote v_2 is visited.
- 4. Choose v_3 from 2 unvisited roots, and first visit E.
- 5. Visit the unvisited child v_1 of v_3 , evaluate, and pebble p_2
- 6. Back to v_3 and pebble p_3

Playing Pebble Game = Deciding Evaluation Order + Variable Recycling



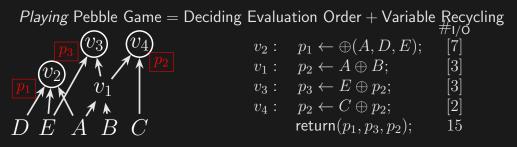
$$v_2: \quad p_1 \leftarrow \oplus (A, D, E)$$

$$v_1: \quad p_2 \leftarrow A \oplus B;$$

$$v_3: \quad p_3 \leftarrow E \oplus p_2;$$

$$v_4: \quad p_2 \leftarrow C \oplus p_2;$$

- 1. Choose v_2 from unvisited roots: alphabetical small $v_2 \prec v_3 \prec v_4$.
- 2. Evaluate the children of v_2 in alphabetical order.
- 3. Put a pebble p_1 on v_2 to denote v_2 is visited.
- 4. Choose v_3 from 2 unvisited roots, and first visit E.
- 5. Visit the unvisited child v_1 of v_3 , evaluate, and pebble p_2
- 6. Back to v_3 and pebble p_3
- 7. Finally, we compute v_4 with moving/recycling pebble p_2 .



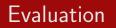
Example: Evaluating strategy based on Depth-first-search

Can we find the best reordering and pebbling in polynomial time?

Theorem (Sethi 1975, Papp & Wattenhofer 2020)

Unless $\mathbf{P} = \mathbf{NP}$, for a given P, in polynomial time, we cannot find a Q that $\llbracket P \rrbracket = \llbracket \overline{Q} \rrbracket$ and minimizes $\#_{I/O}(Q)$.

We use DFS-based strategy as above in our evaluation.



Data Set & Evaluation Environment

We consider RS(10, 4) as an example data set. ▶ We have 1-encoding SLP P_{enc}. ▶ We have ¹⁴ ₄ = 1001 decoding SLPs.

We used two environments in my paper:

name	CPU	Clock	Core	RAM
intel	i7-7567U	4.0GHz	2	DDR3-2133 16GB
amd	Ryzen 2600	3.9GHz	6	DDR4-2666 48GB

In a distributed computation,

our test environments correspond to single nodes.

1 cache specification:	Size	Associativity	Line Size
	32KB/core	8-way	64 bytes

Metric	$Base_{enc}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
#⊕	755	 		
#mem	2265			

	Metric	$Base_{P_{enc}}$	¦ RePa	air	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#⊕	755	 			
	#mem	2265	 			
$\mathcal{B}=512:$	$\#_{\mathrm{I/O}}(K=64)$	570				
$\mathcal{B} = 1 K$:	$\#_{\mathrm{I/O}}(K=32)$	1262	 			
$\mathcal{B} = 2K$:	$\#_{I/O}(K=16)$	1598				

Throughput is Avg. of 1000-runs for 10MB randomly generated data Baco B-Byte Blocking for Cache Efficiency

 $\mathcal{B} =$

 $\mathcal{B} =$

 $\mathcal{B} =$

$$\begin{array}{c|c} & \text{for } i \leftarrow 0 \dots (A \cdot \text{len} / \mathcal{B}) \{ \\ & v_1 = \text{xor}(A, B); \\ & v_2 = \text{xor}(v_1, C, D); \implies v_2^{[i]} = \text{xor}(A^{[i]}, B^{[i]}); \\ & \text{return}(v_1, v_2); \\ & & \\ & \text{return}(v_1, v_2); \\ & \text{where } A^{[i]} \text{ is the } i\text{-th } \mathcal{B}\text{-bytes block.} \end{array}$$

	Metric	$Base_{P_{enc}}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	' 		
	#mem	2265			
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	I I I		
D = 0.012.	Throughput (GB/s)	3.10	 		
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262	r I I		
<i>D</i> – 11(.	Throughput (GB/s)	4.03	 		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598			
	Throughput (GB/s)	4.45			

	Metric	Base P_{enc}	RePair RePair + RePair + Fuse + Why smaller blocks are slower
	_#⊕	755	than the large one?
	#mem	2265	Pros: Smaller blocks,
B = 510.	$\#_{I/O}(K=64)$	570	• More cache-able blocks $\frac{32K}{B}$.
$\mathcal{D} = 012$.	Throughput (GB/s)	3.10	Cons: Smaller blocks,
$\mathcal{B} = 1 \mathbf{k} \cdot$	$\#_{I/O}(K=32)$	1262	 Due to cache conflicts, using cache identically is more
-b = 1 N .	Throughput (GB/s)	4.03	difficult.
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	 Latency penalty becomes totally large.
	Throughput (GB/s)	4.45	

	Metric	$Base_{P_{enc}}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	_#⊕	755	385		
	#mem	2265	1155		
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	 		
D = 012.	Throughput (GB/s)	3.10	! !		
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262			
$\mathcal{D} = \Pi \mathcal{C}$	Throughput (GB/s)	4.03	 		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598			
	Throughput (GB/s)	4.45	 		

	Metric	Base P_{enc}	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	385		
	#	2265	1155		
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231		
$\mathcal{D} = 012$.	Throughput (GB/s)	3.10	 		
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262	1465		
<i>D</i> – IR .	Throughput (GB/s)	4.03	 		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599		
	Throughput (GB/s)	4.45	 		

	Metric	$Base_{P_{enc}}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	385		
	#mem	2265	1155		
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231		
D = 012.	Throughput (GB/s)	3.10	4.18		
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262	1465		
D = 1 K .	Throughput (GB/s)	4.03	4.36		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599		
	Throughput (GB/s)	4.45	4.86		

	Metric	$Base_{P_{enc}}$	RePair	_{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	385	N/A	
	#mem	2265	1155	677	
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231		
D = 0.012.	Throughput (GB/s)	3.10	4.18		
$\mathcal{B} = 1 \mathbf{k} \cdot$	$\#_{I/O}(K=32)$	1262	1465		
D = 1 K .	Throughput (GB/s)	4.03	4.36		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599		
	Throughput (GB/s)	4.45	4.86		

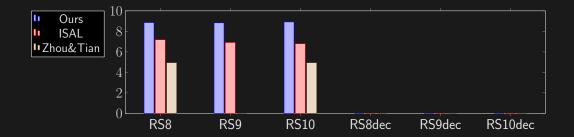
	Metric	$Base_{P_{enc}}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	385	N/A	
	#	2265	1155	677	
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231	936	
$\mathcal{D} = 012$.	Throughput (GB/s)	3.10	4.18		
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262	1465	1086	
D = 1 K .	Throughput (GB/s)	4.03	4.36		
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599	1144	
	Throughput (GB/s)	4.45	4.86		

	Metric	Base P_{enc}	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#	755	385	N/A	
	#	2265	1155	677	
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231	936	
$\mathcal{D} = 012$.	Throughput (GB/s)	3.10	4.18	6.98	
$\mathcal{B} = 1 \mathbf{K} \cdot$	$\#_{I/O}(K=32)$	1262	1465	1086	
D = IK.	Throughput (GB/s)	4.03	4.36	7.50	
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599	1144	
	Throughput (GB/s)	4.45	4.86	7.12	

Metric		$Base_{P_{enc}}$	RePair	^{RePair} + Fuse	RePair + Fuse + Pebbling
	#⊕	755	385	N/A	
	#mem	2265		677	
$\mathcal{B} = 512:$	$\#_{I/O}(K=64)$	570	1231	936	636
	Throughput (GB/s)	3.10	4.18	6.98	7.24
$\mathcal{B} = 1 K$:	$\#_{I/O}(K=32)$	1262	1465	1086	779
	Throughput (GB/s)	4.03	4.36	7.50	8.92
$\mathcal{B} = 2K:$	$\#_{I/O}(K=16)$	1598	1599	1144	845
	Throughput (GB/s)	4.45	4.86	7.12	8.55

Throughput Comparison (Intel + 1K-Blocking)

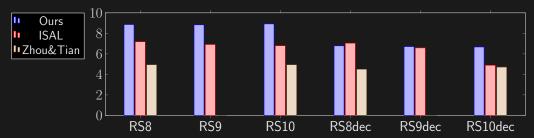
Enc	#mem	#ı/o	Ours	ISA-L v2.30	Zhou & Tian
RS (8, 4)	543	585	$8.86~\mathrm{GB/s}$	$7.18~\mathrm{GB/s}$	$4.94~\mathrm{GB/s}$
RS (9,4)	611	671	8.83	6.91	N/A in their paper
RS (10, 4)	677	779	8.92	6.79	4.94



Throughput Comparison (Intel + 1K-Blocking)

Enc	#mem	#ı/o	Ours	ISA-L v2.30	Zhou & Tian
RS (8, 4)	543	585	$8.86~\mathrm{GB/s}$	$7.18~\mathrm{GB/s}$	$4.94~\mathrm{GB/s}$
RS (9,4)	611	671	8.83	6.91	N/A in their paper
RS (10, 4)	677	779	8.92	6.79	4.94

Dec	#mem	#ı/o	Ours	ISA-L v2.30	Zhou & Tian
RS (8, 4)	747	811	$6.78~\mathrm{GB/s}$	$7.04~\mathrm{GB/s}$	$4.50~\mathrm{GB/s}$
RS (9,4)	829	968	6.71	6.58	N/A
RS (10, 4)	923	1077	6.67	4.88	4.71



Conclusion (+ Other Throughput Scores)

intel 1K	Ours		ISA-L v 2.30		Zhou & Tian	
(GB/sec)	Enc	Dec	Enc	Dec	Enc	Dec
RS (8,3)	12.32	8.82	9.09	9.25	6.08	5.57
RS(9,3)	11.97	8.27	7.31	7.92	6.17	5.66
RS (10, 3)	11.78	8.89	6.78	7.93	6.15_{S}	5.90
RS (8,2)	18.79	14.59	12.99	13.34	8.13_{E}	8.07_{E}
RS(9,2)	18.93	14.27	11.85	12.03	8.34_{E}	8.04
RS(10, 2)	18.98	14.66	12.12	12.61	8.40_{E}	8.22_{E}

Conclusion

- ▶ We identified bitmatrix multiplication as straight line programs (SLP).
- We optimized XOR-based EC by optimizing SLPs using various program optimization techniques.
- Each of our techniques is not difficult; however, it suffices to match Intel's high performance library ISAL.
- As future work on cache optimization, I plan to accommodate multi-layer cache L1, L2, and L3 cache.